CLAIMS

1. A semiconductor device comprising:

a terminal test circuit for testing a state of a contact of an external terminal; and

a test mode control circuit unit for outputting a signal indicating a first operation mode when a power supply voltage is applied thereto, for outputting a test mode signal to said terminal test circuit in response to a control signal input to a specific terminal in said first operation mode, and for outputting a signal indicating a second operation mode in response to the number of times in which the level of the control signal input to said specific terminal changes.

2. A test circuit according to claim 1, wherein said first operation mode is a terminal test mode and said second operation mode is a normal operation mode.

3. A semiconductor device according to claim 2,

wherein said specific terminal is a chip select terminal, and

wherein upon application of a chip select signal of an active level to said chip select terminal in said terminal test mode, said terminal test circuit is activated.

4. A semiconductor device according to claim 3,

wherein said terminal test circuit includes a plurality of circuits for carrying out a plurality of types of test, and

wherein said test mode control circuit unit selectively activates any one of said plurality of the test circuits in accordance with the number of times in which said chip select signal has become an active level from the time when said terminal test mode is assumed.

5. A semiconductor device according to claim 3,

wherein said terminal test circuit is set to a non-select state thereby to assume said normal operation mode when said chip select signal of an active

level is applied thereto a predetermined number of times in said terminal test mode.

6. A semiconductor device according to claim 4, wherein said terminal test circuit is set to a non-select state thereby to assume said normal operation mode when said chip select signal of an active level is applied thereto a predetermined number of times in said terminal test mode.

7. A method of testing a semiconductor device comprising the steps of:

applying a control signal having an active level to said specific terminal of one of a plurality of semiconductor devices mounted on a substrate according to claim 1; and

carrying out a terminal connection test on said selected one of the semiconductor devices

8. A semiconductor device according to claim 4, wherein said circuit for carrying out plural kinds of tests at least includes:

a first test circuit for confirming the state of the contact of any input terminal other than said chip select terminal; and

a second test circuit for confirming the state of the contact of at least a data input/output terminal.

9. A semiconductor device according to claim 3, wherein said chip select terminal is connected to a power supply line through a predetermined load.

10. A semiconductor device according to claim 2, further comprising:

a power supply terminal exclusively used for a data output circuit unit for outputting a test result in said terminal test mode; and

a starter for generating a starter signal upon detection of the application of a power supply voltage to said power supply terminal dedicated to said

data output circuit unit;

wherein said test mode control circuit unit assumes said terminal test mode in response to said starter signal.

11. A method of testing a semiconductor device having a first group of terminals and a second group of terminals, comprising the steps of:

applying a power supply voltage to said semiconductor device;

carrying out a first test for activating a test circuit for checking a state of a contact of the terminals of said first group by supplying a chip select signal having an active level to said semiconductor device and thereby checking the state of the contact of the terminals of said first group; and

carrying out a second test for checking the state of the contact of the terminals of said second group by restoring said chip select signal to an inactive level and reactivating said chip select signal, thereby activating the test circuit for checking the state of the contact of the terminals of said second group.

12. A testing method according to claim 11, further comprising the step of:

repeating the operation of activating said chip select signal as many times as the number of the terminal groups of said semiconductor device after switching on power.

13. A method of testing a semiconductor device comprising the steps of:

applying a power supply voltage to a power supply terminal of said semiconductor device;

carrying out a first test for checking a state of a contact of a chip select terminal and said power supply terminal by supplying said chip select signal to a chip select terminal in said semiconductor device;

carrying out a second test for checking

the state of the contact of any input terminal other than said chip select terminal by restoring said chip select signal to an inactive level and reactivating said chip select signal and activating a test circuit for confirming the state of the contact of said input terminal; and

carrying out a third test for checking the state of the contact of at least a data input/output terminal by restoring said chip select signal to an inactive level followed by reactivating said chip select signal, and then activating the test circuit for checking the state of the contact of said data input/output terminal.

14. A semiconductor integrated circuit comprising:

a first external terminal and a second external terminal each connected to an internal circuit;

a test mode control circuit unit activated in response to an application of a power supply voltage thereto, and outputting a test mode signal in response to a control signal applied to said first external terminal, said test mode control circuit unit being deactivated when the logic level of said control signal changes a predetermined number of times; and

a terminal test circuit unit connected to said second external terminal for determining a state of a contact of said second external terminal in response to said test mode signal.

15. A semiconductor integrated circuit according to claim 14,

wherein said first external terminal is an input terminal of a chip select signal.

16. A semiconductor integrated circuit according to claim 14, further comprising:

a pull-up resistor for pulling up said control signal to the level of said power supply voltage.

17. A semiconductor integrated circuit according to claim 14, further comprising:

an external data terminal; and

a data output circuit unit for outputting read data to said external data terminal;

wherein said power supply voltage is supplied to said data output circuit unit.

18. A semiconductor integrated circuit according to claim 14, further comprising:

an external data terminal; and

a data output circuit unit for outputting read data to said external data terminal;

wherein said test mode control circuit unit outputs a first test mode signal in response to a first activation edge of said control signal and outputs a second test mode signal in response to a second activation edge of said control signal;

wherein said terminal test circuit unit is activated in response to said second test mode signal; and

said data output circuit unit outputs a signal corresponding to the level of said first test mode signal from said external data terminal in response to said first test mode signal, and outputs a test signal from said terminal test circuit unit to said external data terminal in response to said second test mode signal.

19. A semiconductor integrated circuit according to claim 18, further comprising:

a data input circuit unit for receiving input data applied to an external data terminal;

wherein said test mode control circuit unit outputs a third test mode signal in response to a third activation edge of said control signal;

wherein said data input circuit unit outputs said input data to said data output circuit unit in response to said third test mode signal; and

wherein said data output circuit unit outputs said input data to said external data terminal in

response to said third test mode signal.

20. A semiconductor integrated circuit according to claim 19,

wherein said data output circuit unit outputs an input signal to said external data terminal asynchronously with a clock in response to said first, second and third test mode signals.

21. A semiconductor integrated circuit according to claim 18,

wherein said test mode control circuit unit outputs a fourth test mode signal in response to an activation period thereof, and said output data circuit unit selectively receives a normal input signal and a test input signal in response to said fourth test mode signal.

22. A semiconductor integrated circuit according to claim 19,

wherein said test mode control circuit unit outputs a fourth test mode signal in response to an activation period thereof, and said output data circuit unit selectively receives a normal input signal and a test input signal in response to said fourth test mode signal.

23. A semiconductor integrated circuit according to claim 14,

wherein said second external terminal includes a plurality of external terminals, and said terminal test circuit unit determines whether or not a signal of one of logic levels is input to one of said plurality of external terminals and a signal of the other logic level is input any one of to the other external terminals.

24. A semiconductor integrated circuit according to claim 14,

wherein said test mode control circuit unit includes:

a latch circuit which is reset in response

to an application of said power supply voltage thereto;

a switch interposed between a first node and an input terminal of said latch circuit for carrying out on/off operations in response to said control signal;

a second node connected to an output terminal of said latch circuit; and

a gate circuit for outputting said test mode signal during a period in which the logic levels of said first and second nodes coincide with each other.